A 0.9V 20.9dBm 22.3%-PAE E-Band Power Amplifier with Broadband Parallel-Series Power Combiner in 40nm CMOS

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The 71-to-76GHz and 81-to-86GHz bands (known as E-band) exhibit low atmospheric attenuation and are allocated by FCC and CEPT for long-haul transmission. They enable multi-Gb/s fixed-link services such as fiber extension/replacement and cellular backhaul. It is beneficial to have a device operating in both 5GHz bands for high data throughput (due to full usage of the 5GHz band) and low interference (due to the 10GHz spacing between two bands). This requires a PA that delivers uniform gain and output power from 71 to 86GHz. An output power of more than 20dBm is also desired for sufficient link margin to accommodate rain attenuation. These requirements are not satisfied by prior reported 70/80GHz PAs in silicon-based technology [1-4].

This paper reports a fully integrated 40nm CMOS PA that utilizes a broadband parallel-series power combiner to achieve an output power (P_{OUT}) of 20.9dBm with more than 15GHz small-signal 3dB bandwidth (BW_{3dB}) and 22% PAE at 0.9V supply. The in-band variation of P_{1dB} is only ±0.25dB. This silicon-based PA covers both 71-to-76GHz and 81-to-86GHz bands with uniform gain, output power and PAE.

Transformer-based series combiners are popular in mm-Wave PA design due to their high power transfer efficiency and compact layout. However, two crucial issues limit the efficiency and effectiveness of such structures to combine more than four signal paths (i.e., two differential signal paths) to achieve high output power at mm-Wave. 1) The parasitic interwinding capacitance between the primary and secondary coils will distort the amplitude and phase of the signals to be combined and reduce the combining efficiency. 2) The input impedance in each path of the series combiner decreases in proportion to the number of the combining paths. Considering that the performance of mm-Wave transistors is constrained by the loss of the peripheral intraconnects, the typical value of the transistor width above 60GHz is limited to 100 to 150µm, which leads to an optimum load impedance (Z_{OPT}) of a common-source (CS) differential amplifier in the range of 30 to 50Ω. Therefore, to accomplish beyond 2-way differential combining, either the transistor size needs to be considerably increased for a much lower Z_{OPT} (i.e., causing much higher intraconnect loss) or an additional matching circuit is required to perform the impedance transformation. The above two issues will limit the output power, combining efficiency and bandwidth of the whole network.

In this design, a combination of parallel and series combiners is used, which efficiently combines four differential amplifiers with low insertion loss and at the same time minimizes the impedance transformation ratio of the whole passive network to maximize the bandwidth. Figure 14.1.1 shows the E-band PA schematic that incorporates two unit PAs with a slow-wave T-line-based parallel combiner. Each unit PA consists of two neutralized CS amplifiers and a transformer-based series combiner. The slow-wave T-line in the parallel combiner has a differential-mode characteristic impedance of 79Ω. It transforms the 50Ω load (100Ω seen by each differential T-line) and pad parasitics to an equivalent resistance of 52Ω seen by the two unit PAs. The series combiner reduces the impedance by a factor of 2 and provides the Z_{OPT} (i.e., 28Ω, close to half of 52Ω) for the output stage. With this parallel-series power combining approach, the transistor size of each PA stays optimal for high power gain and efficiency, while four of these PAs are combined efficiently with low impedance transformation ratio as required for broadband operation. Figure 14.1.2 plots the power contours of the output stage at 74 and 83GHz and the input impedance of series combiner (i.e., Z_{OPT} seen by the output stage) from 70 to 95GHz. It is shown that optimum power matching is achieved in the entire band. The load resistance maintains around 28Ω and the load inductance increases at lower frequency which is desired for broadband matching. The insertion loss of the complete parallel-series combiner is less than 1dB from 65 to 86GHz.

The broadband power matching for the drivers will be constrained by the interstage matching network. Therefore, the driver stage is sized sufficiently large to provide enough linear power for the output stage in the 71-to-86GHz band. In this design, each driver drives two output stages and they have the same transistor size (176µm/40nm). The transistor layout is optimized to minimize the intraconnect loss. Compared to the PDK transistor model, the maximum power gain of the neutralized CS amplifier is reduced by only 0.7dB (C_N=43fF). In addition, the parallel T-line-based power divider at the input also lowers the overall input impedance by a factor of 2, which simplifies the input matching design and preserves the bandwidth.

A compact floor plan is crucial to mm-Wave circuits where the placement of all the interconnects has to be considered carefully. These interconnects should not only route the signals between stages but also be employed as part of the matching circuits to minimize the overall loss. Besides, the unwanted magnetic coupling that cannot be avoided in a compact design has to be characterized accurately. Figure 14.1.3 illustrates the layout of the output series combiner, the power divider and associated interconnects. The distance between the combiner and divider is only 34.2µm. There are two ways to connect the power divider and the output stages, referred as interconnects A and B in Fig. 14.1.3. Both differential interconnects act as part of matching circuits and are optimized to minimize the imbalance and associated loss. The major difference of using these two interconnects is the polarity of coupling between the power combiner and power divider. Simulations predict that the complete PA achieves 1.7dB higher gain with interconnect A and it even outperforms the case when no coupling exists.

The PA prototype is fabricated in a 40nm bulk CMOS process. The chip micrograph is shown in Fig. 14.1.7. Due to the compact floor plan, the chip occupies only 0.19mm² including the input and output RF pads. Thanks to the parallel combining/splitting structures at the PA output/input, the two unit PAs are perfectly symmetrical against the central dashed line. This facilitates the TX integration as the magnetic couplings of the two unit PAs to the preceding stages will be cancelled and the VCO pulling can be alleviated.

Figure 14.1.4 shows the measured small-signal S-parameters. The PA achieves a peak S_{21} of 18.1dB at 78.5GHz and small-signal BW_{3dB} of 15.2GHz (70.3 to 85.5GHz). The S_{11}, S_{22} and S_{12} are lower than -8, -10 and -37dB respectively from 71 to 86GHz. The amplifier is unconditionally stable over the entire measured frequency range (0.1 to 110GHz). Consuming 375mW from a 0.9V supply, the PA has a measured P_{1dB} of 17.4dBm, P_{SAT} of 20.4dBm with 22% PAE_{MAX} at 80GHz. Figure 14.1.5 shows that the PA achieves a measured P_{1dB} of 17.55±0.25dBm, P_{SAT} of 20.55±0.35dBm and PAE_{MAX} of 20.5±1.8% from 71 to 86GHz. The variation of P_{1dB} is even smaller than that of P_{SAT} thanks to the design techniques discussed, which maximize the bandwidth of the output combiners and ensure sufficient power delivered by the drivers. The measured EVM in the 70GHz band (f_c=74GHz) is also shown in Fig. 14.1.5. The input data generated by the AWG and external SSB up-convertor limit the performance. The PA achieves 2Gb/s 16QAM and 5Gb/s QPSK at 12.5 and 13dBm average P_{OUT} respectively with a measured EVM slightly higher than the one directly measured from the setup. For long-term reliability, we operated the PA with 20dBm P_{OUT} at 0.9V for more than 10 hours. No obvious degradations of output power (<0.1dB) and drain current (<1%) were observed.

Figure 14.1.6 summarizes the comparison with the state-of-the-art 70/80GHz PAs in silicon. This work achieves comparable small-signal BW_{3dB} to a distributed topology [3] that compromises in efficiency and silicon area. Among the PAs in the comparison table, the proposed 0.19mm² CMOS PA achieves highest and nearly uniform P_{1dB}, P_{SAT} and PAE_{MAX} in the 71-to-86GHz band at 0.9V supply.

Acknowledgments:
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[2] J. Oh, B. Ku, S. Hong, "A 77-GHz CMOS Power Amplifier with a Parallel Power Combiner Based on Transmission-Line Transformer," *IEEE Trans. on Microwave Theory and Techniques*, vol. 61, pp. 2662-2669, July 2013.

[3] E. Afshari et al., "Electrical Funnel: A Broadband Signal-Combining Method," *ISSCC Dig. Tech. Papers*, Feb. 2006.

[4] M. Thian, M. Tiebout et al., "A 76-to-84GHz SiGe Power Amplifier Array Employing Low-Loss Four-Way Differential Combining Transformer," *IEEE Trans. on Microwave Theory and Techniques*, vol. 61, no. 2, pp. 931-938, Feb. 2013.

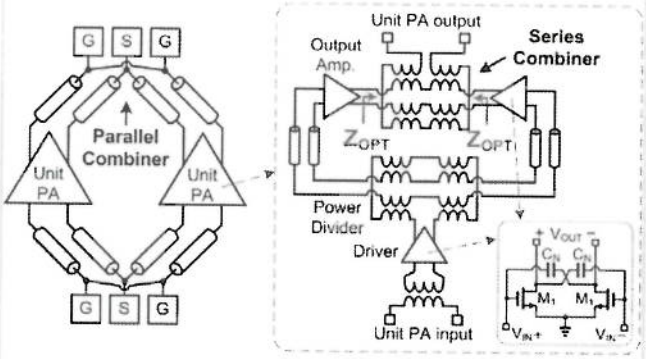


Figure 14.1.1: Schematic of the complete PA and the unit PA.

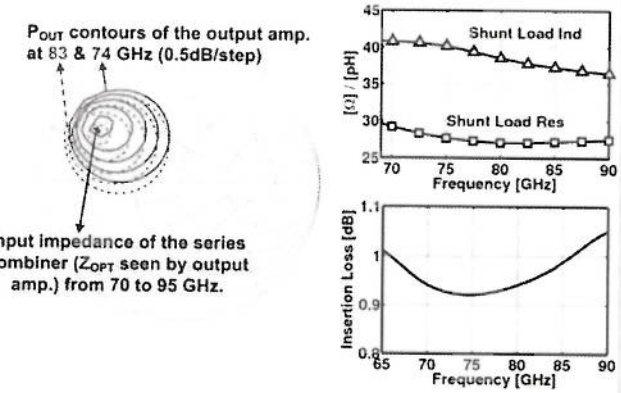


Figure 14.1.2: Input impedance of the series combiner and the simulated insertion loss of the parallel-series combiner (including output pads).

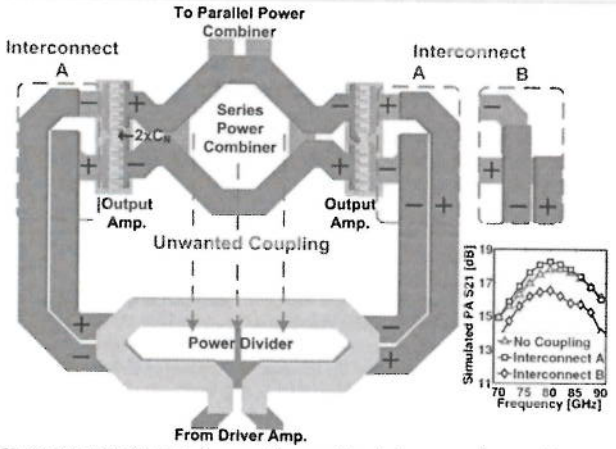


Figure 14.1.3: Unwanted magnetic coupling between series combiner and power divider (supply and ground lines not shown for simplicity but included in the simulation) and simulated S_{21} of the complete PA with different coupling effects.

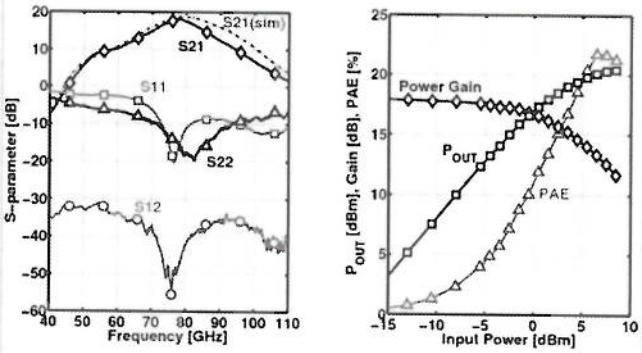
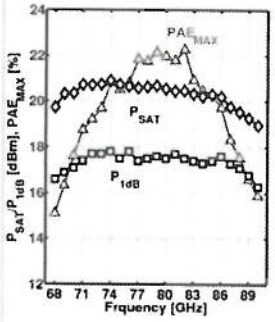


Figure 14.1.4: Measured S-parameters vs. frequency and measured power gain, output power, PAE vs. input power at 80GHz.



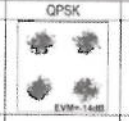
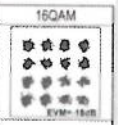
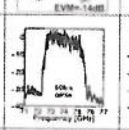
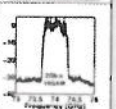
Modulation	QPSK	16QAM
Constellation [2048 points]		
Spectrum [dB]		
Data Rate	5Gb/s	2Gb/s
EVM	-14dB	-18dB
EVM of setup	-16dB	-18.5dB
Average P_{OUT}	13dBm	12.5dBm

Figure 14.1.5: Measured P_{SAT}, P_{1dB} and PAE_{MAX} vs. frequency, and measured EVM (w/ & w/o DUT) in 70GHz band (f_c=74GHz).

	This Work	K-Y. Kang ISSCC12 [1]	J. Oh TMTT13 [2]	E. Afshari ISSCC06 [3]	Y. Zhao JSSC12	A.Y-K Chen TMTT13	M. Thian TMTT13 [4]
Technology	40nm CMOS	65nm CMOS	65nm CMOS	130nm SiGe	130nm SiGe	180nm SiGe	180nm SiGe
V_{DD} [V]	0.9	1.0	2	-2.5/0.8	2.5	4	3.2
Freq. [GHz]	70.3-85.5	79	77	85	84	83	78
Max. S_{21} [dB]	18.1	24.2	20.9	9	27	25	18.3
S_{21} BW$_{-3dB}$ [GHz]	15.2	10	N/A	>18‡	8	9.6	8.9 (BW$_{-2}$)
P_{1dB} [dBm]	17.8	16.4 #	13	N/A	16	12.5	12.5
P_{1dB} variation [dB] Freq. range [GHz]	0.5 71-87	N/A	2 75-82	N/A	2 75-90	1 75-88	N/A
P_{SAT} [dBm]	20.9	19.3 #	15.8	21	18	14.7	14
P_{SAT} variation [dB] Freq. range [GHz]	0.7 69-86	N/A	2.3 75-82	3 74-90	1.5 75-90	1 75-88	4 76-84
PAE_{MAX} [%]	22.3	19.2 #	15.2	4 (Drain Eff)	9	8.1	2
Area [mm²]	0.19	0.855	0.21	2.4†	0.68†	0.34	0.85
Topology* Path combined	2-stage CS 4-way diff.	4-stage CS 8-way	2-stage CA 2-way diff.	DA /CA 4-way	3-stage CB 2-way diff.	2-stage CA 2-way	2-stage CA 4-way diff.

The loss of the on-chip output balun (> 1.6dB) was de-embedded from the measured P_{SAT}, P_{1dB} and PAE_{MAX}.
‡ The gain is only shown from 72 to 90 GHz. † Include the area of DC pads.
* CS: common source, CB: common base, CA: cascode, DA: distributed amplifier.

Figure 14.1.6: Comparison of PAs in 70/80GHz bands.